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ABSTRACT:

For the physical design of a VLSI chip a method is provided to implement a high density master image that contains logic and RAMs. In a hierarchical top-down design methodology the circuitry to be contained on the chip is logically devided into partitions that are manageable by the present automatic design systems and programs. Global wiring connection lines are from the beginning included into the design of the different individual partitions and treated there in the same way as circuits in that area. Thus the different partitions are designed in parallel. A floorplan is established that gives the different partitions a shape in such a way that they fit together without leaving any space between the different individual partitions. The chip need no extra space for global wiring and the partitions are immediataly attached to each other. The master image described is very flexible with respect to logic, RAM, ROM and other macros, and it offers some of the advantages of semicustom gate arrays and custom macro design. The thus designed chip shows no global wiring avenues between the partitions and has partitions of different porosity.

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(54) **Method for physical VLSI-chip design.**

(57) For the physical design of a VLSI chip a method is provided to implement a high density master image that contains logic and RAMs. In a hierarchical top-down design methodology the circuitry to be contained on the chip is logically devided into partitions that are manageable by the present automatic design systems and programs. Global wiring connection lines are from the beginning included into the design of the different individual partitions and treated there in the same way as circuits in that area. Thus the different partitions are designed in parallel. A floorplan is established that gives the different partitions a shape in such a way that they fit together without leaving any space between the different individual partitions. The chip need no extra space for global wiring and the partitions are immediataly attached to each other. The master image described is very flexible with respect to logic, RAM, ROM and other macros, and it offers some of the advantages of semicustom gate arrays and custom macro design. The thus designed chip shows no global wiring avenues between the partitions and has partitions of different porosity.

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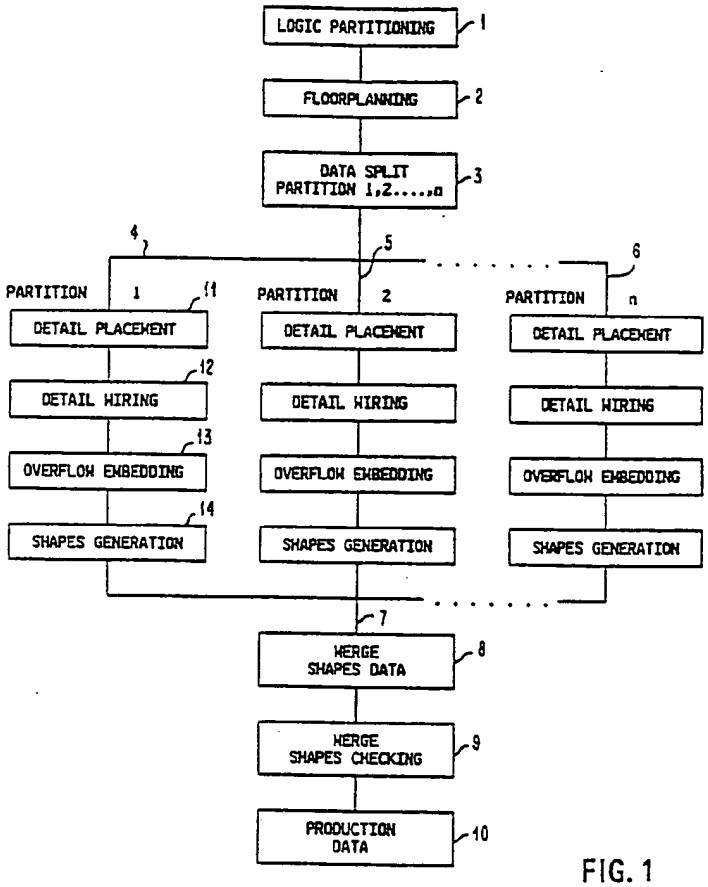
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PARTITION 1
PARTITION 2
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SHAPES GENERATION
SHAPES GENERATION
SHAPES GENERATION
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MERGE
SHAPES DATA
8
MERGE
SHAPES CHECKING
9
PRODUCTION
DATA
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FIG. 1

Method for Physical VLSI-Chip Design

The present invention relates to a method for physical chip design, wherein the chip is devided in several partitions and contains a high number of electrical elements, as for example gates, pins, connections, and wherein connections exist between that partitions.and to a chip designed in accordance with this method.

In the IBM Technical Disclosure Bulletin Vol 27 No.8, January 1985, page 4648 - 4651 there is described a method for functional partitioning of a large, dense VLSI (Very Large-Scale Integration) chip. Described is the physical partitioning of logical functions in the VLSI chip design to keep the wire length of the interconnections between the different partitions as short as possible. This article describes especially an algorism for hierarchical deviding a logical function into more primitive logic functions that are subordinted the higher one.

A further article in the IBM Technical Disclosure Bulletin Vol 27 No. 11, April 1985, pages 6687 - 6691 shows also, that a single chip might be partitioned into regions that might have different electrical and logical functions respectively such as for example elements such as RAM (Random Access Memory) and ROS (Read Only Storage) partitions of PLA's (Programmable Logic Arrays) and other functional partitions. Between those different partitions buses for signal interconnections and power supply are provided.

In an article "Channel Assignment for Chip Wiring" in IBM Technical Disclosure Bulletin Vol. 26 and No.3A, August 1983, pages 934 - 936 the problem of routing global wires between different partitions of a chip is shown. It is said there that a general strategy for wiring chips is to treat the problem into 2 phases: a global assignment of wires is made to specific channels;next, the particular channel tracks for individual wires ae chosen and interconnections established to specified pins on the macros in the chip. A macro essentially can be considered to be a sort of a functional partition.

The problem with presently designed logic and micro-processor chips is that they contain logic circuits in the range of up to 35000 electrical circuits. This huge amount of circuits causes very severe problems during physical design of the chip. The data volume is by far to high to be handled by the available placement, wiring and checking programs runing on a large main frame computer.

One possible way of at least improving this problem might be to use a system architecture with extented memory address capability. But even if the data volume problem is manageable by this architecture, there is still the problem of the run time. That means that the whole execution may be longer than the mean time between failures. Therefore, besides the question that the methodology has not been proved yet, there is the increasing need for run time.

Another principle way of approaching this problem is to partition the whole design complex, performing the design in parallel for so-called macros and then using extra space between the partitions for global wiring. That means on the other hand that the chips size gets larger and that the wire length of the global wires become longer. Longer wires have a direct impact on the performance of the chip and the power dissipation.

It is the principle object of the present invention to provide a way and a methodology for physically designing a VLSI chip by which the overeral chip density can significantly be improved and at the same time the data volume can be handled by existing computers and design programs.

It is also an object of the present invention to provide a method by which it is avoided to need extra space between partitions for global wiring.

Furthermore it is an object of the invention to provide a method that achieves logic circuit densities which compare favourably with those of custom designed chip.

These and other objects are favourably resolved by applying the characterizing features as laid down in main claim 1.

The method in accordance with this invention provides in an advantageous manner a hierarchical physical design methodology in a top-down way. The complete logic circuitry is partitioned logically into pieces that are manageable by computer programs and computers. Those partitions are selected such that the interconnections between them are minimized. The areas of the partiones are shaped such that they fit together without leaving empty space in between. So by a floorplaning no dedicated area is assigned for global wiring. A partition is a self-contained piece of logic, i.e. all connections needed to interconnect neighbouring partitions are included in the partition. That means that one partition may contain wires that emerge, wire that end and wire that cross the partition. All those wires and connections are treated in the same way. For that purpose the connections between the partitions is done by field connectors that consist out of transfer books which provide the necessary contacts. Those transfer books then cooperate with associated transfer books of the neighbouring partitions.

Further with the method in accordance of the invention in advantageous manner of a further de-

velopment the internal layout of the individual partition is performed independently of the layout and design of the other partitions after pin determination of each partition has been performed.

This also means, that in advantagous manner in accordance with the present invention each partition, in a way forming a subchip, can be designed independently from the other partitions and in parallel to it. As result, placement and wiring programs have only to deal with data volumes that are comparable to those associated with single chips or singly macros respectively. This is done regardless of the sizes and complexity of the complete chip. The detailed design of each partition accommodates all the chip features or partition features respectively within its bounderies, for example powergrid and blockages. After all partitions have been designed they are then assembled simply by abuting them at their bounderies. Then only at the outer perimeter of the assembled chip that means the compiled partitions, outer pins connect the chip to its substrate carrier.

A further advantage of the method in accordance with the invention is, that the complete method is interactive and permites a designer to do the physical design of a complex chip in an reasonable amount of time. The logic circuit density achieved compare favourably with those of custom designed chips, while simultaneously applying automated design methodologies.

Further objects and advantages will be come apparent form the sub claims as well as from the following detailed description of an embodiment of the present invention. Reference is made to the accompaning drawing in which

Fig. 1 is a schematic flow chart showning the essential steps of the method in accordance with the present invention;

Fig. 2 shows in principle how the total desgn circuitry is logically devided into separate partitions.

Fig. 3 shows schematically a floorplanning matrix and

Fig. 4 shows an example of the result of a floorplan.

The physical design process coveres the placement and interconnection of all logic gates and custom macros, as well as the generation of shapes data for the production masks. The process or method respectively itself is a highly automated combination of interactive and background steps. Depending on the density and performance requirements it allows a variety of procedures from a fast walk through to a rather extensive method with reiterative steps in order to achieve the objects and goals.

In accordance with the invention a hierarchical top-down methodology is implemtented for the physical design which solves the data volume problem and limits the resource requirements for computer time and storage requirements tremendeously. Actually the exponential growth of computer time is limited to the amount that is required for the largest partition. From there it is a linear growth depending on the number of partitions. The storage requirement is also limited to the size that is required for the largest partition.

Fig. 1 shows the overall flow in subsequent steps of the total physical design method.

In step 1 the total design circuitry is devided by logic partitioning into separate partitions. In step 2 a floor planing step transfers the logic partitions into physical partitions, generating real size and offset coordinates for each partition. After floorplanning is completed the data are separated in order to form single partitions 1,2,...,n in step 3.

In parallel branches of which branch, 4, 5 and 6 are shown the partition 1, partition 2 and partition n are designed in parallel. As shown with branch 7 the result comes together in a step 8 for merging the shapes data. In step 9 those datas are checked and in step 10 out of the checked merged data production data for the masks are generated.

Fig. 2A and 2B show in more detail the logic partitioning as indentified by step 1 in Fig. 1. The total design circuitry 21 as shown Fig. 2A is partitioned for example into segments or partitions respectively A, B, C, D, E, F. Those partitions may contain 3000 - 6000 logic gates. The logic partitioning is performed to form the segments such that the number of connections between the different functional islands or segments A to F is minimized. That means, resulting logic partitions have a minimum number of connections runing from one partition to the other partitions, those connections are indicated by double arrows in Fig. 2B. Such partitions then have a defined number of inputs/outputs and meet the maximum partition limits.

With regard to Fig. 3 and Fig. 4 the floorplanning step 2 (see Fig. 1) is described in more detail. A floorplanning matrix is shown with 400 positions. Within those 400 positions for example the twelve shown partitions A - M have to be placed. That means that the logic partitions A - M (see for example the functional islands shown in Fig. 2B as example) have to be transferred into physical partitions. In the floorplanning step the best partition arrangement in relative positions to each other is sought. That means with other words that in this step the real size and th offset coordinates of each partition within the available chip area is generated. In addition to that it is taken care that access to the periphery I/O circuits and all required signal interconnections to other partitions is given. The partition areas are definged in a way that they fit together seamless like pieces of a puzzle. No

extra space for global wiring is defined in the resulting floorplan nor intended to.

To overcome the need for global wiring routing avenues running around the different partitions, all required interconnections between the different partitions do run as feed-through-connections through the different partitions from one partition to the partition where they should run to. Internally in each partition those global wires crossing the boundaries are handled as if they where parts of this partition. That means that beside ending and emerging lines from a partition also the crossing lines are treated equally. Equally with circuits in that area. In result the global wires are routed straight through the partitions, thus allowing the shortest possible connection lenght. That on the other hand means that within a partition the internal circuits are arranged more to the edges of the partiton and the feed-through-connections lines run through the middle of the partition. That also means that some areas of a partition are denser packed as others and no equal density is given. By choosing the porosity of an area in accordance with necessity, a very flexible design is given.

Fig. 4 shows a result of the physical floorplanning. It shows the puzzle-like and seamless putting togehter of the different partitions A - M.

To allow subsequent processing in a physical design using standard design automation programs, for each partition transfer circuits or transfer books are added to the logic structure of each partition. These transfer circuits or transfer books represent just wiring channel crosspoints at the partition bounderies. This means each signal or wire entering or leaving a partition gets at least one of those transfer circuits. For example a horizontal feed through connection is represneted by just two transfer circuits, one at the right side and one at the left side of the partition. Within the automatic wiring procedure the corresponding transfer circuits (left to right) are connected. The resulting wire forms a feed-through-connection.

If is ist necessary in floorplanning for blocking out some areas with in a partition, formal transfer books can be created. Those formal transfer books are adjacent to the real transfer books and the logic transfer books.

Decisive is that from the beginning global wires crossing a partition are treated in the same way as circuits on that specific partition and be considered as a part of this partition.

After having completed the floorplanning, the resulting data are seperated in order to form single partitions. Each of these partitions is than processed like a seperate chip through physical design programs. As shown in branch 4 of Fig. 1 there is a step 11 for detail placement of the first partition. The phase of detail placement is optimized to meet the requirements of the subsequent wiring phase. These requirements mainly are a homogenious distibution of points to be wired over the full partition area and to supply a sufficient number of free wiring channels for feed-through-connections.

During the detail placement step 11 within each partition the following placement tagets are important: the overall wiring length has to be minimized and any clustering has to be avoided. An even distubution of wiring points and a balanced center and edge density is aimed on. Furthermore, space has to be provided for bus structures as well as for feed-throughs, that means crossing lines. Also the critical net capability has to be obayed.

As the floorplanning process of step 2 takes care of all required connections, the space allocation for each partition has been adjusted accordingly in order to allow the placement to reach this objective. As a result the partitions located near the chip center will have a lower circuit density than partitions located near the chip periphery. During the floorplanning step 2 the space calculation in accordance to known values is important. Critical points are the number of circuits, the density factor and the numbers of connections. Furthermore, the population factor at the center and at the edge of a partition and especially the feed-through-connection.

After the first partition 1 is processed through placement, in the detail placement step 11, the next adjacent partition, for example partition 2 in Fig. 1 or considering the floorplanning result of Fig. 4 partition H adjacent to partition A, can be started with detail placement. The only difference to the first partition A is, that the transfer circuits located on their common boundry, that means at the line 41, must be processed as preplaced for the second partition now. Exits on line 41 from partition A are inputs to partition H. That means that a partially overlapped processing for all partitions is possible.

After detail placement a step 12 in Fig. 1 provides the detail wiring for each partition. A standard chip wiring program is used to automatically complete the connection of all circuits, transfer circuits and transfer books as well as embedded macros as usual.

In the detail wiring step 12 during which circuits within each partition have to be connected, the overall wiring length has to be minimized. Furthermore even wiring channel usage is sought for. The number of overflows should be minimized and an easy embedding should be aimed at.

For very dense parts a small number of connections may be left as overflows. In this case an interactive tool is used to complete the remaining connection at the screen in the overflow embedding step 13.

In step 14 the shapes generation for each partition can be performed. This is done after detail wiring is completed and final checks are successfully processed. Then, in the shape generation step 14, the shapes for the production masks are generated.

As shown in step 8 of Fig. 1 branch 7 combines the shapes data of the different partitions. In a final merge run the shapes data of all partitions are collected and put together. Each partition has its own XY offset according to the floorplan. On the bounderies of the partitions the transfers bokks of adjacent partitions are overlaid. Because these transfer books represent wiring channel cross points, the wiring pieces of the puzzle snap together and complete nets are formed matching the overall logic structure.

In step 9 an extensive final checking is performed on the emerged shape data. This completes the physical design process. In this checking the partition data are checked against the total image data. In addition, especially the connection data for signals crossing partition bounderies are checked for completeness and the partition bounderies are checked for overlap conflicts. Finally out of these checked data the production data are generated in step 10.

The method in accordance with the present invention is very flexible with respect to logic, RAM, ROM and other macros. It describes a master image. Macros of any size can be placed at any location on the chip. The method was implemented with a technology using for the master image a 1.0 µm CMOS N-Well structure with three layers of metal. Two layers are used for wiring and the third layer contains a power distribution and I/O redistribution for the central area pad arrangement.

The master image is an array of cell locations without gates or transistors. The virtual cell grid is subdivded in a finer grid marking the vertical and horizontal wiring channels. The cell size might be for example 13.8 µm x 89 µm. This basic cell contains at most 3 pairs of transistors and provides 25 wiring channel on the 1st level and 3 channels on the 2nd level metal. 2 channels on the 1st level maybe blocked by powerlines. To meet all groundrule restrictions imposed by any wiring and via combination, the circuit layouts have to harmonize with the wiring grid. This is achieved by placing sub-circuit elements on the same grid and connect into pieces with standard wires ofpolysilicon, 1st and 2nd metal. A logic circuits blocks 3 - 5 channels on 1st level metal by its internal connections. During personalization the logic circuits, represented by books, and the larger macros which might be custom designed, are placed and wired by the automatic design system. A single circuit represented by a book may take the area of one or more cells. Macros like RAM's are custom designed parts with an optimized layout.

The used master image in accordance with the present invention is suitable for circuit depopulation achieved by the placement strategy. During the placement procedures the chip areas showing a congestion of global interconnections are identified. They are depopulated by moving the circuits toward the peripheries of these areas. Empty cells in the center yield the required routing channels. Thus a uniform and therefore optimal usage of the wiring channels is achieved. It also means, that the offering of a considerable amount of about 30 % more cells then actually can be used was done purposely in order to allow the depopulation. The power buses are distributed on special, some what wider channels forming a low inductive grid on 1st and 2nd level metal. They are conntacted frequently to the 3rd level metal buses. The supple current is flowing mainly through these wide and therefore low ohmic and low inductive distribution nets on the 3rd level metal rather than through 1st and 2nd metal. These can be cut out anywhere for embedding of any sized macro. The macros provide there own local power distribution which is connected directly to the 3rd level metal.

The method in accordance with the present invention for the physical design of the master images of VLSI chips combines the advantage of gate arrays and full custom designs. This method is very flexible for integration logic books, RAM, ROS and other macros. Different areas of the chip can be designed in parallel thus reducing the necessary computer time and computer storage requirements. As wiring connections between the different areas or partitions respectively of the chip are included in the design of the individual partitions, the resulting chip needs no extra space for global wiring. Thus a chip results with seamless attached and separately designed areas. Design changes in the individual partitions can be performed easily and without imparting the rest of the design.

Claims

1. Method for physical chip design, said chip being divided in several partitions and containing a high number of electrical elements e.g. gates, pins, connections etc., wherein connections exist between said partitions, characterized in that

a) circuits to be placed on said chip are logically divided into partitions;

b) said logic partitions are chosen such that they contain a number of circuits taht are manageable, e.g. by a computer and computer programs;

c) said partitions, after determining th ir space requirements, are placed onto differenet areas of said chip,

d) determining all partition crossing lines, i.e. global wiring,

e) determining logic as well as crossing, ending and emerging connection lines within a partition,

f) treating connection lines within each of said partitions in the same way as circuits, and establishing interconnection information for the edges of said partitions, and

g) shaping the partitions so that they fit to each other without leaving space inbetween in the neighbouring edges of said adjacent partitions, and

h) attaching the appropriatly shaped partitions seamlessly to each other,

2. Method as of claim 1, wherein
after pin determination of each of said partitions the internal layout of said individual partition is performed independently of the layout and design of the other partitions.

3. Method as of claim 1 or 2, wherein
the pin data or pin location respectively of crossing, ending or emerging connection lines located at the edges of a partition are handled in the same way as input/ output information of a usual chip layout design process.

4. Method as of claim 3, wherein
normal chip design programs are used in designing each of said individual partitions.

5. Method in accordance with one or several of the preceding claims, wherein
the circuit package density of each of said partitions is accomodated to the number of connection lines crossing, emerging or ending in said specific partition, so that a variable porosity of said individual partition is provided.

6. Method for physical chip design, said chip being divided in several partitions and containing a high number of electrical elements, e.g. gates, pins, connections, etc., wherein connections exist between said partitions, characterized in that

a) all circuits going to be contained on the chip are divided logically in several partitions;

b) a floorplan that reflects space requirements as well as locations of said partitions is established;

c) interconnect-points whereever needed are generated at the edges of said partitions;

d) said partitions are processable independently and in parallel considering at the same time the internal circuits as well as interconnection lines that cross, emerge or end in said partition; and

e) said partitions are implanted such on the spacial area of the chip that they fit together at adjacent edges without leaving space inbetween, that associated interconnect-points match each other, that maximum utilization of the whole spacial area is reached, wiring congestion is avoided, and for heat dissipation and wiring length an optimum is provided.

7. Method as of claim 6, wherein
each one of said partitions, that may differ in size and shape, are further dividable into subareas, e.g. regions, for improving wireability and for limiting processing time.

8. Method as of claim 6 or 7, wherein
wiring and checking of said specific partitions and/or regions respectively is performable in parallel.

9. Method as of claim 6, 7 or 8, wherein
the density or porosity respectively of partitions/regions is adjustable/variable.

10. Method as in one of claims 6 to 9, wherein
in the middle of a region/partition the density of crossing interconnection lines is chosen higher than in the outer areas of that respective region/partition, and the density of circuits is chosen to be higher in the outer areas of that respective region/partition than in the middle.

11. Method in accordance with one of the claims 6 to 10, wherein
the determining of interconnect contact points at the boundaries of partitions is performed by starting in one specific area of the chip, for example the left upper corner, and propagating step-by-step into orthogonal directions, for example to the right and downwards, thus exit information and contact areas of one partition form the input information or placement respectively for the succesive adjacent partition or partitions respectively, and so on.

12. Method in accordance with one of the preceding claims, wherein
transfer books with logical functions, provided by electrical circuits, as well as transfer books with non-logical functions, provided by connection and transfer wires, are established, both sort of books adjacent at the perimeter of its respective partition and defining the boundary interconnect-contact areas.

13. Method in accordance with claim 12, wherein
books are assigned to blockage areas, for example for buses, arrays, gates those books having formal functions, and existing during processing for design purposes and being resolvable in the final design stage.

14. Chip containing a very large number of electrical elements, for example circuits, gates, pins, connections etc., and being divided in several partitions that are interconnected by interconnection lines, characterized in that

a) said partitions are intimately attached to each other at their respective adjacent edges leaving no space inbetween;

b) said partitions contain interconnect-contact pins at their boundaries/edges that connect crossing interconnection lines from edge to edge with matching interconnect-points at the adjacent partition and emerging and ending interconnection lines in matching fashion as well as said electrical elements, and

c) said partitions are of different porosity, i.e. one partition might by packed more densly than the other.

15. Chip as in claim 14, wherein the boundaries/edges of said partitions form straight lines.

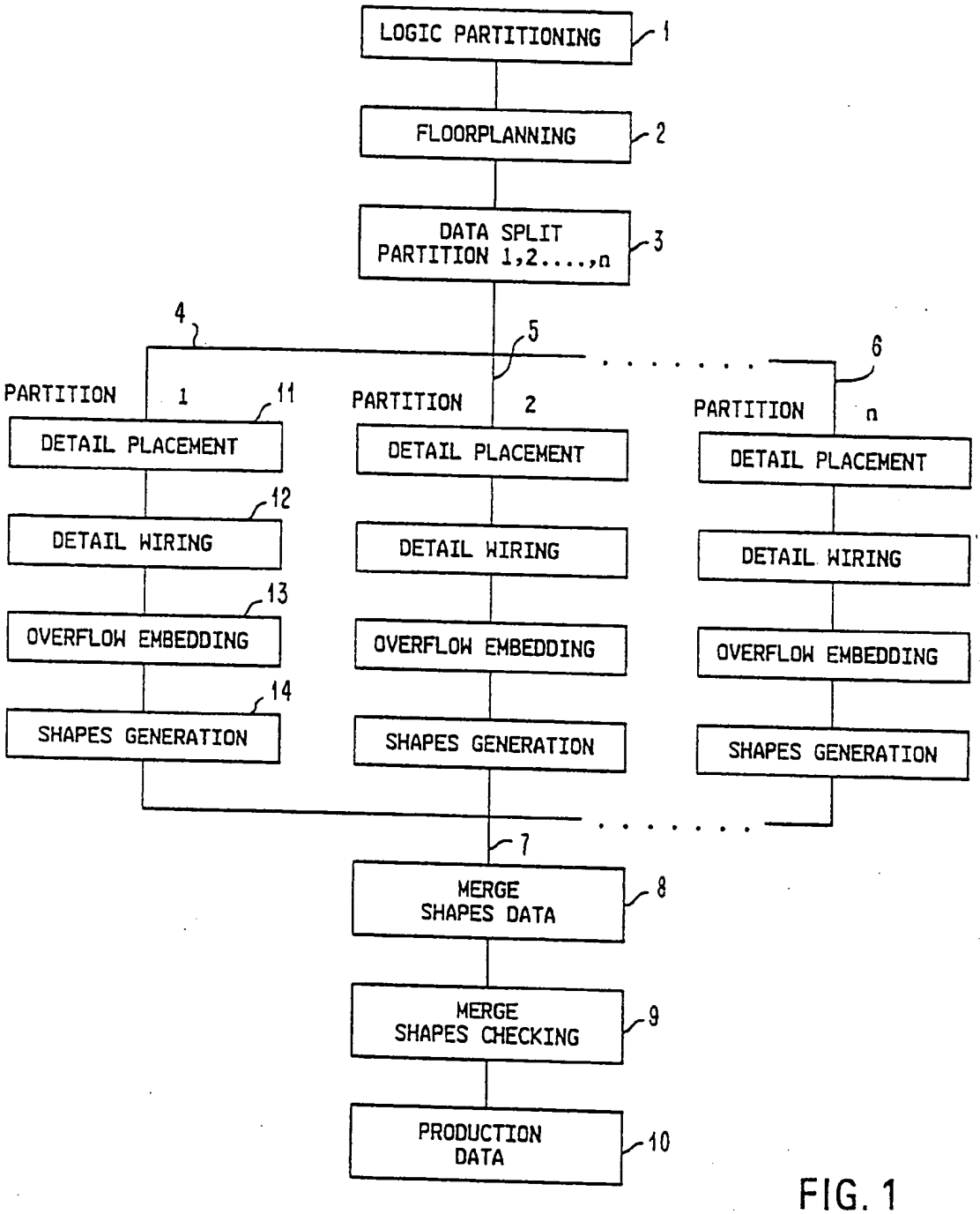
LOGIC PARTITIONING
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FIG. 1

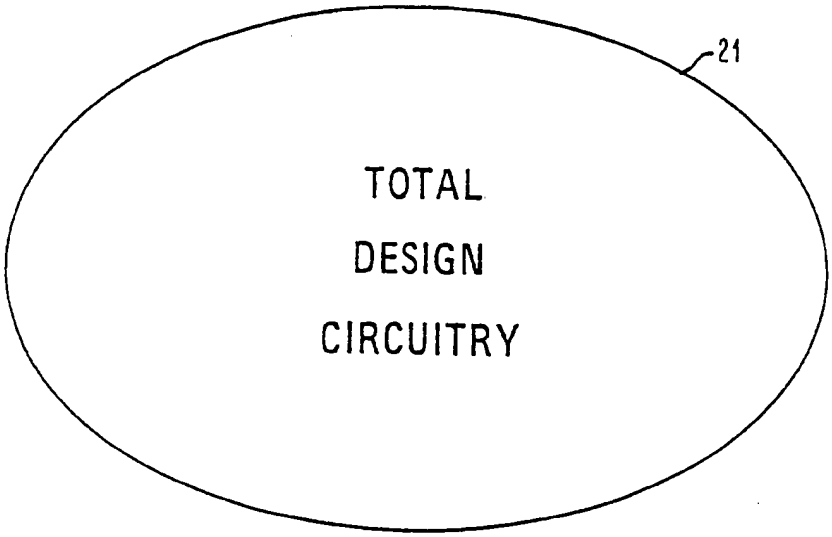

FIG. 2A

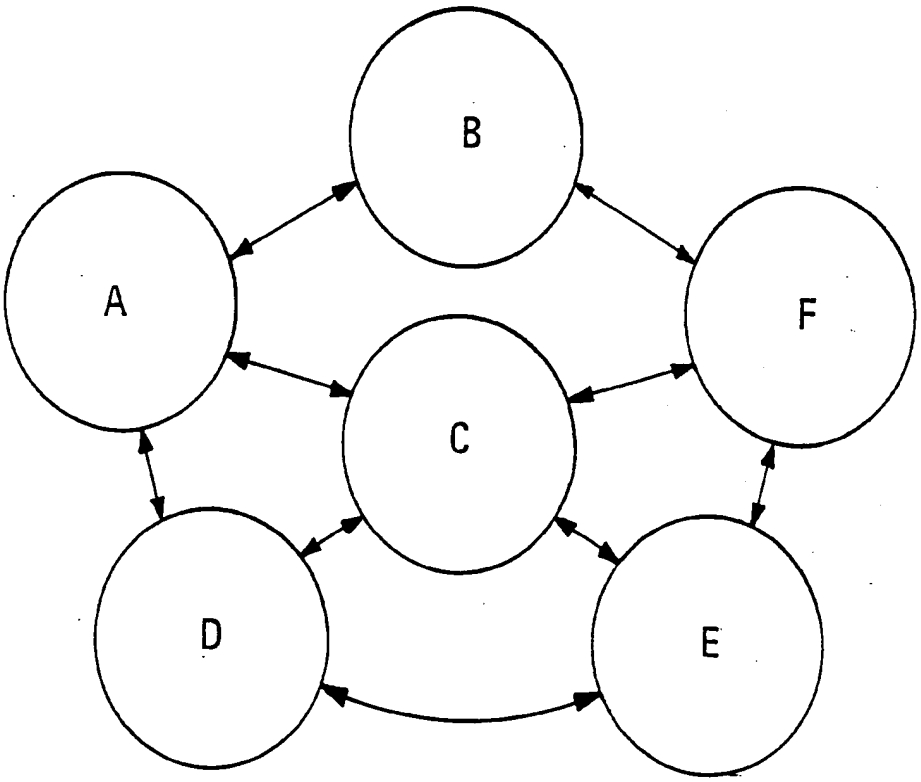

FIG. 2B

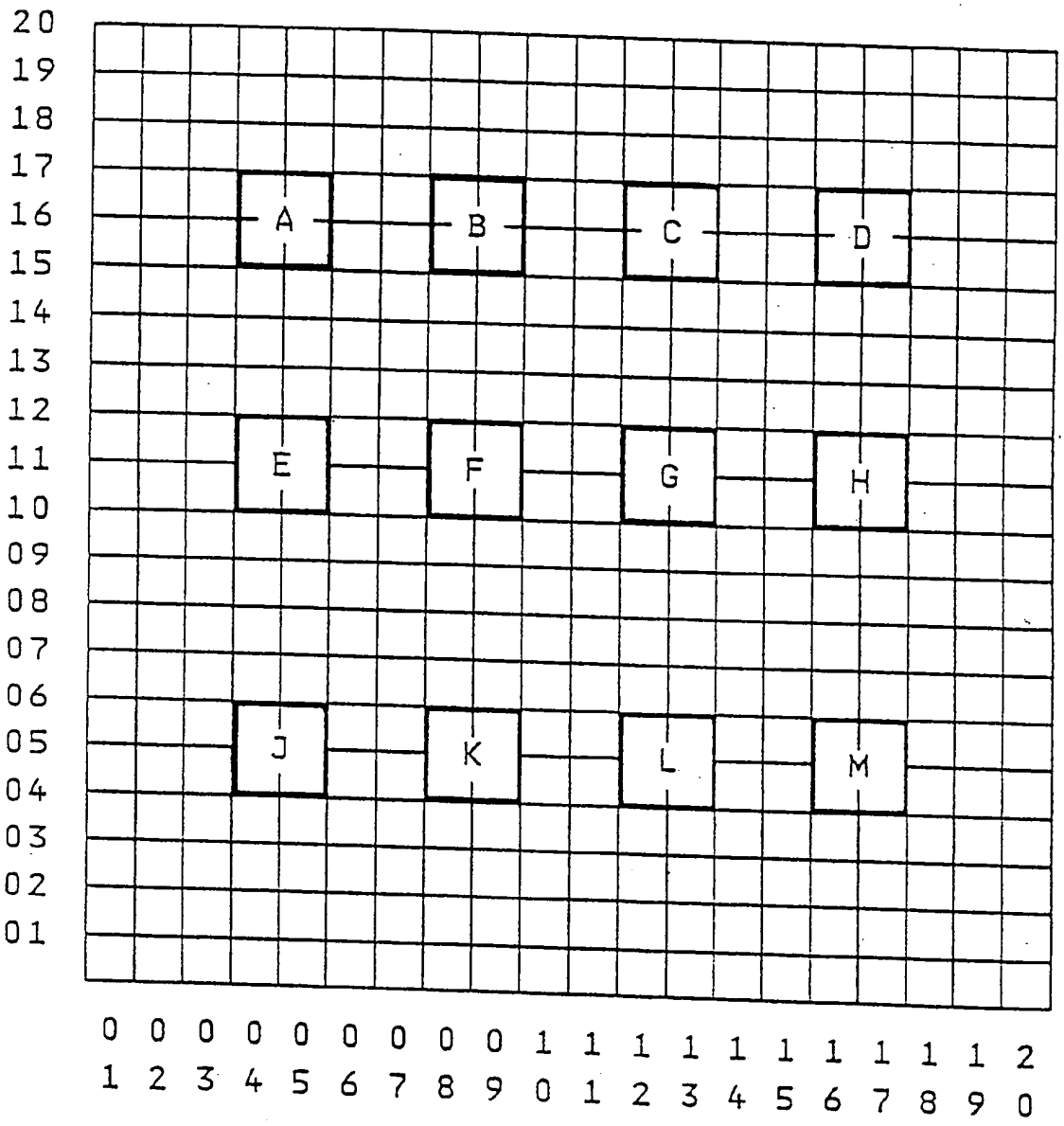
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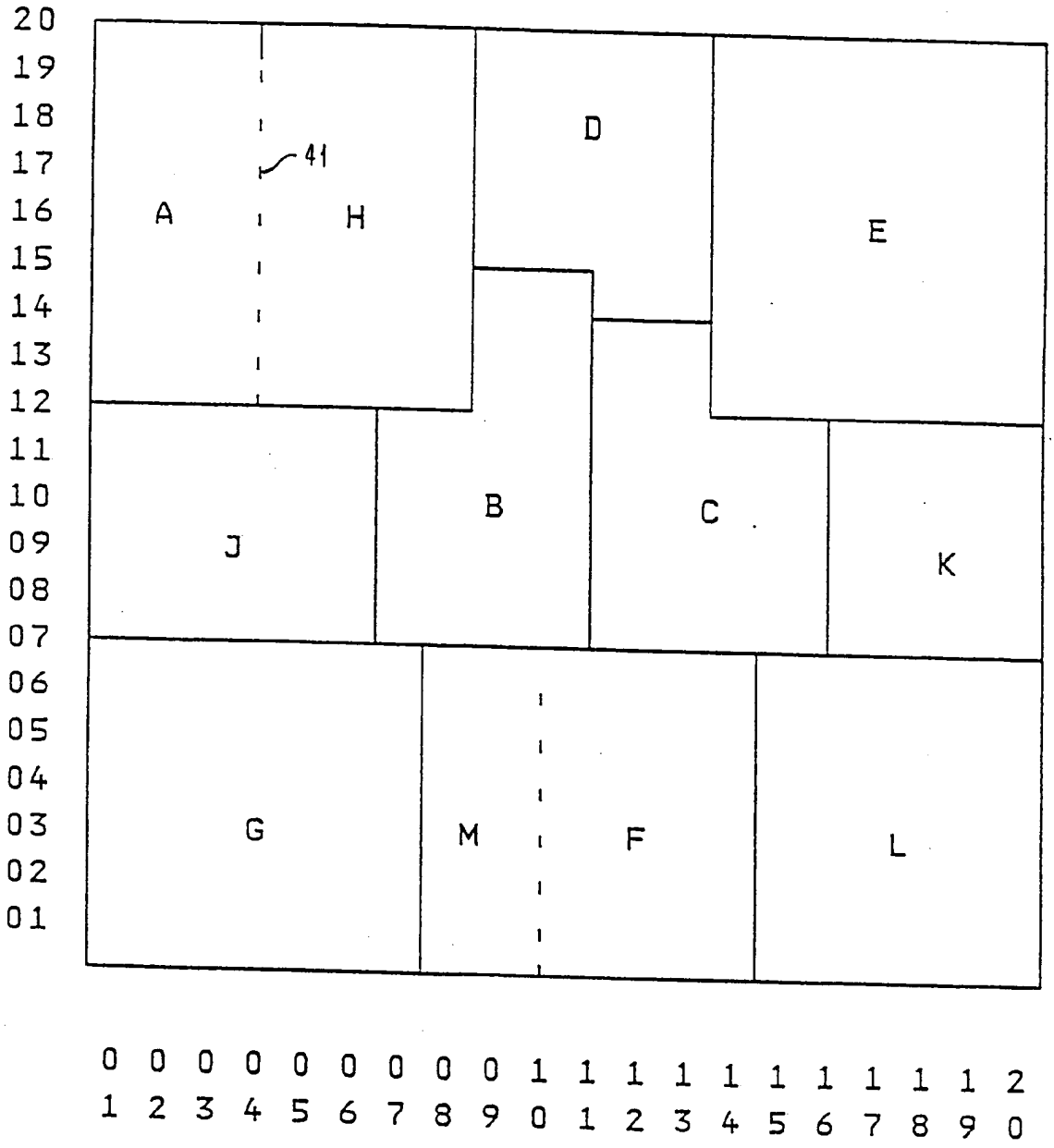
FIG. 3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1 2 3 4 5 6 7 8 9 0 1 2 3 4 5 6 7 8 9 0

FIG. 4

European Patent Office

EUROPEAN SEARCH REPORT

Application number

EP 86 11 7601

DOCUMENTS CONSIDERED TO BE RELEVANT

Category	Citation of document with indication, where appropriate, of relevant passages	Relevant to claim	CLASSIFICATION OF THE APPLICATION (Int. Cl.4)
A	ELECTRONICS & COMMUNICATIONS IN JAPAN, vol. 68, no. 2, part II, March-April 1985, pages 37-46, Scripta Technica, Inc., Silver Spring, Maryland, US; HIROSHI YOSHIMURA et al.: "Hierarchical and automatic layout design method for logic VLSI" ---		G 06 F 15/60
A	IEEE TRANSACTIONS ON AUTOMATIC CONTROL, vol. AC-28, no. 6, June 1983, pages 671-677, IEEE, New York, US; M.A.BREUER et al.: "A methodology for custom VLSI layout" ---		
A	PROCEEDINGS OF THE IEEE INTERNATIONAL CONFERENCE ON COMPUTER DESIGN: VLSI IN COMPUTERS, Sponsored by IEEE Computer Society and IEEE Circuits and Systems Society, ICCD'85, Port Chester, New York, 7th-10th October 1985, pages 63-67, IEEE Computer Society Press; TSUNENORI UMEKI et al.: "A prototype microcontroller design by symbolic layout approach" -----		TECHNICAL FIELDS SEARCHED (Int. Cl.4) G 06 F 15/60

The present search report has been drawn up for all claims

Place of search	Date of completion of the search	Examiner
THE HAGUE	07-07-1987	BURGAUD C.

CATEGORY OF CITED DOCUMENTS

X : particularly relevant if taken alone
Y : particularly relevant if combined with another document of the same category
A : technological background
O : non-written disclosure
P : intermediate document

T : theory or principle underlying the invention
E : earlier patent document, but published on, or after the filing date
D : document cited in the application
L : document cited for other reasons

& : member of the same patent family, corresponding document

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Entwicklung und Forschung

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18 May 1987

Anmelderin/Applicant: International Business Machines
Armonk, N.Y. 10504, USA

Anmeldung Nr./
Application No.: GE 986 013

Zeichen/Ref.: 86 117 601.4

In reply to the letter of 4 May 1987, please find enclosed an attachment containing a list of corrections, presented in the requested form with references to the passages to be corrected in which way.

Therefore, this letter and its attachment is considered to be the request under Rule 88 EPC as asked for.

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Encl.
Attachment (threefold)

ATTACHMENT
to our reply to the Communication
of 4 May 1987 concerning European Patent
Application 86 117 601.4 (Ref. GE 986 013)

18 May 1987

Please correct the above mentioned patent application as follows:

Page 1, Para. 1, Line 2
Instead of "is devided in several"
It should read "is divided into several"

Page 1, Para. 1, Line 5
Instead of "that partitions,"
It should read "those partitions,"

Page 1, Para. 2, Line 8
Instead of "deviding"
It should read "dividing"

Page 1, Para. 3, Line 2
Instead of "pages 6687 - 6691 shows also,"
It should read "pages 6687 - 6691 shows,"

Page 1, Para. 3, Line 3, 4
Instead of "regions that might have different electrical and logical functions respectively such as for example"
It should read "with different logical functions for example"

Page 1, Para. 3, Line 8
Instead of "power supply"
It should read "power supplies"

Page 2, Para. 1, Line 4
Instead of "It is said there that"
It should read "The article says that"

Page 2, Para. 1, Line 5, 6
Instead of "is to treat the problem into 2 phases:"
It should read "is to solve the problem within phases:"

Page 2, Para. 1, Line 8
Instead of "interconnections established"
It should read "interconnections are established"

Page 2, Para. 2, Line 3
Instead of "35000 electrical circuits. This huge"
It should read "35000. This huge"

Page 2, Para. 2, Line 4
Instead of "problems during physical design"
It should read "problems during the physical design"

Page 2, Para. 3, Line 6
Instead of "mean time"
It should read "meantime"

Page 2, Para. 4, Line 3
Instead of "so- called"
It should read "so-called"

Page 2, Para. 4, Line 4
Instead of "partitions for global"
It should read "macros for global"

Page 2, Para. 4, Line 5
Instead of "chips size"
It should read "chip size"

Page 2, Para. 4, Line 6
Instead of "become"
It should read "becomes"

Page 3, Para. 3, Line 3
Instead of "chip"
It should read "chips"

Page 3, Para. 5, Line 8
Instead of "So by a floorplanning"
It should read "So, by floorplanning"

Page 3, after Para. 5, insert the following paragraph:
"With other words:
Formal transfer circuits without a logic function are introduced. Their pins define the input output positions at the partition boundary. Those transfer circuits then cooperate with associated transfer circuits of the neighbouring partitions. The transfer circuits act like a connector, which connects the global wires between adjacent partitions. During partition wiring all wires are treated simultaneously in the same way."

Page 4, Para. 2, Line 1
Instead of "that in advantageous manner"
It should read "that in an advantageous manner"

Page 4, Para. 2, Line 4
Instead of "in parallel to it."
It should read "in portions parallel to them."

Page 4, Para. 2, Line 6
Instead of "associated with single chips"
It should read "associated with today's single LSI chips"

Page 4, Para. 2, Line 7, 8
Instead of "regardless of the sizes and complexity of the complete chip"
It should read "regardless of the size and complexity of the complete VLSI chip"

Page 4, Para. 3, Line 3
Instead of "permites"
It should read "permits"

Page 4, Para. 3, Line 4
Instead of "in an reasonable amount"
It should read "within a reasonable amount"

Page 4, Para. 3, Line 5
Instead of "compare"
It should read "compares"

Page 4, Para. 3, Line 6, 7
Instead of "while simultaneously applying automated design methodologies" it should read "while the application of automated design methodologies reduces the design time."

Page 5, Para. 5, Line 3, 4, 5
Instead of "The process or method respectively itself is a highly automated combination of interactive"
It should read "The design method consists of a combination of highly automated interactive "

Page 6, Para. 1, Line 5, 6
Instead of "After floor- planning is completed the data are separated in order to"
It should read "After floorplanning is completed the data is separated to"

Page 6, Para. 2, Line 3
Instead of "comes"
It should read "come"

Page 6, Para. 2, Line 4, 5
Instead of "those datas are"
It should read "the shapes are"

Page 6, Para. 2, Line 5, 6
Instead of "step 10 out of the checked merged data production data"
It should read "step 10 production data"

Page 6, Para. 3, Line 8
Instead of "That means, resulting logic"
It should read "That means, the resulting logic"

Page 7, Para. 2, Line 11
Instead of "lenght."
It should read "length."

Page 7, Para. 2, Line 15
Instead of "partition are denser packed"
It should read "partition are packed denser"

Page 8, Para. 1, Line 2, 3
Instead of "circuits or transfer books are added"
It should read "circuits are added"

Page 8, Para. 1, Line 4
Instead of "These transfer circuits or transfer books represent"
It should read "The pins of these transfer circuits represent"

Page 8, Para. 2, Line 1 - 4
"If is ist necessary in floorplanning for blocking out some areas with in a partition, formal transfer books can be created. Those formal transfer books are adjacent to the real transfer books and the logic transfer books."

shall be replaced by following paragraph:
"A partition must keep all its circuits and all wires inside the area for this partition. A formal circuit without logic function is introduced. It is placed all around the partition area and blocks all wiring channels within its occupied area. So during physical design of the partition all circuits and wires are forced to stay inside the partition area."

Page 8, Para. 4, Line 1, 2
Instead of "floorplanning, the resulting data are separated"
It should read "floorplanning, the data is separated"

Page 9, Para. 4, Line 1
Instead of "placement a step 12"
It should read "placement a step 11"

Page 11, Para. 2, Line 16, 17
Instead of "These can be cut out anywhere for embedding of any sized macro."
It should read "The power buses on first and second metal can be cut out anywhere for embedding macros of any size."

Page 12, Para. 1, Line 4
Instead of "for integration logic books,"
It should read "for integration of logic books,"

Page 12, Para. 1, Line 8
Instead of "partitions respectively of the chip"
It should read "partitions of the chip"

Page 12, Para. 1, Line 12
Instead of "imparting"
It should read "impacting"

Page 17, Para. 2, Line 1- 4
"books are assigned to blockage areas, for example for buses, arrays, gates, those books having formal functions, and existing during processing for design purposes and being resolvable in the final design stage."

shall be replaced by following paragraph:
"formal blockage circuits are assigned to blockage areas, for example to keep areas free for buses and arrays, those circuits having formal functions, and existing during processing for design purposes and being removable in the final design stage and final chip data."